UNITED STATES PATENT AND TRADEMARK OFFICE

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10/549,368	09/14/2005	Balakrishnan Srinivasan	NL 030268	2307

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EXAMINER
JOHNSON, BRIAN P

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
	10/549,368	SRINIVASAN ET AL.
Office Action Summary	Examiner	Art Unit
	BRIAN P. JOHNSON	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2005*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-15 have been examined.

2.   Acknowledgement of papers filed: oath/declaration, specification, drawings,

claims on 14 September 2005. These papers filed have been placed on record.

Specification

3.   The title of the invention is not descriptive. A new title is required that is clearly

indicative of the invention to which the claims are directed.

Claim Objections

4.   Claim 14 is objected to under 37 CFR 1.75(c), as being of improper dependent

form for failing to further limit the subject matter of a previous claim. Applicant is

required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper

dependent form, or rewrite the claim(s) in independent form.

        In particular, Claim 12 is drawn to a computer program product, while Claim 14,

which depends on claim 12, is drawn to a method, apparently failing to contain the

computer program product of claim 12.

Claim Rejections - 35 USC § 112

5.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

6.   Claim 10-12 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

The following portion of claim 10 does not appear to make grammatical sense,

therefore it is difficult to asses proper patentable weight of the claim: "in the absence of

instruction to the contrary storing results of the commands in a register file; in the

absence of instruction to the contrary receiving register sourced operands of the

commands from the register file." Please revise.

Claims 11 and 12 are rejected for being dependent on Claim 10.

Claim Rejections - 35 USC § 101

7.   35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
conditions and requirements of this title.

Claims 12 and 15 are rejected under 35 U.S.C. 101 because they are drawn to a

computer program product that are indicated in Applicant's Specification as including

non-statutory subject matter (Specification pages 3 lines 17-19). It is unclear whether

Claim 14 is intended to include the same computer program product limitation due to its

status as an improper dependent. If such a limitation is intended to be included in Claim

14, then it is also rejected under 35 USC 101.

Claim Rejections - 35 USC § 102

8.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9.   Claims 1, 2, 6 and 10-15 are rejected under 35 U.S.C. 102(b) as being

anticipated by Cilvin U.S. Publication No. 2004/0148494.

10.   Regarding Claim 1, Cilvin discloses an instruction processing device comprising

an instruction issue unit for issuing successive instructions (paragraphs 5 and 6); a

plurality of pipe-line stages coupled to the instruction issue unit (paragraph 5), at least

one of the pipe-line stages comprising a functional unit for executing a command from

the instructions (paragraph 5); a first register unit (paragraph 5) coupled to the

functional unit for storing a result of execution of the command when the command has

reached a first one of the pipeline stages (paragraph 5), and for supplying bypass

operand data to a circuit in a pipe-line stage preceding the first one of the pipeline

stages (paragraph 6); a second register unit, coupled to the functional unit for storing

the result when the command has reached a second one of the pipeline stages,

downstream from the first one of the pipeline stages (paragraph 5), and for supplying

operand data to the functional unit; a disable circuit coupled to selectively disable

storing of the results in the second register unit under control of the instructions

(paragraph 13).

11.   Regarding Claim 2, Cilvin discloses an instruction processing device according to

claim 1, wherein the first and second register unit each comprise a plurality of registers

and addressing circuitry for selective addressing with a register address from the

command, for selecting a register for storing the result and/or for retrieving operand

data (paragraph 13).

12.   Regarding Claim 6, Cilvin discloses an instruction processing device according to

claim 2, comprising a bypass control unit arranged to compare a result register address

for the result from a first one of the commands with an operand register address from a

second one of the commands that follows the first one of the commands directly or

indirectly, and to substitute a result from the register of the first register unit that

contains the result for an operand from the second register unit in case of a match of

the addresses (paragraph 6).

13.   Regarding Claim 10, Cilvin discloses a method of executing a program of

instructions in an instruction processor, the method comprising pipelining execution of

commands from the instructions (paragraphs 5 and 6); in the absence of instruction to

the contrary storing results of the commands in a register file; in the absence of

instruction to the contrary retrieving register sourced operands of the commands from

the register file; selectively using a first one of the results bypassed from a pipelining

stage as a bypassed operand instead of at least one of the register sources operands

from the register file (paragraph 11); selectively suppressing, under program control,

writing of the first one of the results to the register file (paragraph 13).

14.   Regarding Claim 11, Cilvin discloses a method according to claim 10, comprising writing the first one of the results into an addressable one of a plurality of bypass registers that are located to receive the result earlier during pipelining than the register file (paragraph 11).

15.   Regarding Claim 12, Cilvin discloses a computer program product comprising instructions for an instruction processor for implementing the method according to claim 10 (paragraph 2).

16.   Regarding Claim 13, Cilvin discloses a method of compiling a program of instructions for an instruction processor, the method comprising generating a series of instructions (paragraph 5); first detecting for a result to be produced by a first one of the instructions which second one of the instructions use the result as operand (paragraph 11); second detecting whether it can be guaranteed that it will be possible to bypass the result in the instruction processor as operand for all second ones of the instructions without retrieving the result from a register file (paragraph 15); generating information in the instruction to disable writing to the register file when it can be guaranteed that it will be possible to bypass the result as operand in the instruction processor for all second ones of the instructions (paragraph 15).

17.   Regarding Claim 14, Cilvin discloses a method of compiling according to claim

12, comprising including an indication in the instructions that the result should be stored

in one of a plurality of bypass registers that is addressable on writing and/or reading of

the result to the plurality of bypass registers (paragraph 11).

18.   Regarding Claim 15, Cilvin discloses a computer program product comprising

instructions for an instruction processor for implementing the method according to claim

13 (paragraph 2).

Claim Rejections - 35 USC § 103

19.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

20.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cilvin in

view of Clock and Power Gating with Timing Closure (herein Mukherjee).

21.   Regarding Claim 4, Cilvin discloses an instruction processing device according to

claim 2, but fails to disclose the remaining limitations.

        Mukherjee discloses gating clocks to save power when registers do not change

value (see generally)

Cilvin would have been motivated to utilize this technique to save power.

It would have been obvious at the time of the invention for one of ordinary skill in the art

to take the processing system of Cilvin and incorporate the clock gating of Mukherjee.

The combination would prevent the temporary register files from being written into the

general register when such a writing is determined not to be necessary.

22.   Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being obvious over Cilvin

in view of Mantor (U.S. Patent No. 6,624,818).

23.   Regarding Claim 7, Cilvin discloses an instruction processing device according to

claim 1, but fails to disclose the remaining limitations.

Mantor discloses that the first register unit comprises a chain of registers (Fig. 13

references 760-780) for supplying bypass operand data, arranged as a shift register

with an input coupled to a result output of the first one of the stages and operative to

shift the result through successive shift register stages in successive instruction cycles,

at least if storing of the result in the second register unit is disabled, the chain extending

further than necessary for writing the result into the second register unit (col 21 lines 5-

65).

Cilvin would have been motivated to utilize this technique to reduce latency

(Mantor col 21 lines 29-32).

It would have been obvious at the time of the invention for one of ordinary skill in the art

to take the processing system of Cilvin and incorporate the bypass register queue of

Mantor.

24.   Regarding Claim 8, Cilvin/Mantor discloses an instruction processing device

according to claim 7, wherein the registers in the chain are addressable from the

commands (Mantor col 21 lines 5 to 65).

25.   Claims 3, 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Cilvin in view of common art.

26.   Regarding Claim 3, Cilvin discloses an instruction processing device according to

claim 2, wherein the first register unit contains fewer registers than the second register

unit.

        Examiner takes Official Notice that the first register unit (pipeline units or latches

mentioned in paragraph 5) generally contain less registers than the second register unit

(a general register file).

        Cilvin would have been motivated to utilize this technique because, in normal

processor operation, a general register requires more storage space than a pipeline

register.

        It would have been obvious at the time of the invention for one of ordinary skill in

the art to have the processing system of Cilvin contain a larger general register file than

a pipeline register.

27.   Regarding Claim 5, Cilvin discloses an instruction processing device according to claim 3, comprising a plurality of functional units, arranged to execute respective commands from an instruction in parallel, the second register unit having a plurality of write ports for writing the result from respective ones of the functional unit, the disable circuit being arranged to disable writing at selected write ports, selected under control of the instructions.

Examiner takes Official Notice that it is common in the art to have multiple functional units and write ports for general registers.

Cilvin would have been motivated to utilize this technique to improve parallelization and, therefore, improve the efficiency of the processor.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Cilvin and incorporate multiple functional units and write ports to the register files. It would follow, for proper program execution, that only certain write ports would be suppressed when limiting the write back function of the processing system.

28.   Regarding Claim 9, Cilvin discloses an instruction processing device according to claim 2, comprising a functional unit (paragraph 5), arranged to execute respective commands from an instruction, the first register unit comprising respective groups of registers, the registers of all groups being addressable from the command for retrieving an operand.

Cilvin fails to disclose that there are multiple functional units. Official Notice is

taken similar to that of Claim 3. Additionally, Official Notice is taken that particular

functional units are given sets of register specific to that functional unit.

Cilvin would have been motivated to utilize this technique to improve the ease of

programming and data coherency inside the processor.

It would have been obvious at the time of the invention for one of ordinary skill in the art

to take the processing system of Cilvin and incorporate functional unit specific register

files.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a

rejection of claims in an application or patent under reexamination, the applicant or

patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments

avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Brian P Johnson whose telephone number is (571) 272-

2678. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4174. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183